Hysteresis in Single-Layer MoS_2 Field Effect Transistors

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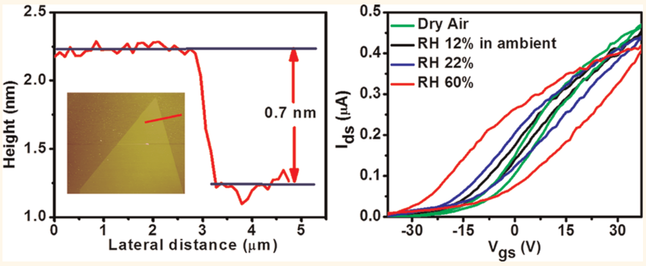
ABSTRACT



Field effect transistors using ultrathin molybdenum disulfide (MoS_2) have recently been experimentally demonstrated, which show promising potential for advanced electronics. However, large variations like hysteresis, presumably due to extrinsic/environmental effects, are often observed in MoS_2 devices measured under ambient environment. Here, we report the origin of their hysteretic and transient behaviors and suggest that hysteresis of MoS_2 field effect transistors is largely due to absorption of moisture on the surface and intensified by high photosensitivity of MoS_2. Uniform encapsulation of MoS_2 transistor structures with silicon nitride grown by plasma-enhanced chemical vapor deposition is effective in minimizing the hysteresis, while the device mobility is improved by over 1 order of magnitude.

KEYWORDS: molybdenum disulfide · field effect transistor · hysteresis · photosensitivity · moisture · silicon nitride · PECVD

Graphene has attracted considerable interest in the past few years because of its extraordinary linear dispersion for charge carriers and other unique physical properties, which originate from its low dimensionality.[1−3] However, zero band gap of graphene limits its application in semiconductor devices.[4,5] Recently, other layered materials such as molybdenum disulfide (MoS_2) have received renewed interest due to the possibility of creating atomically thin films with nonzero band gap.[5−13] Structurally similar to graphite, MoS_2 is built up of atomic planes held together by weak van der Waals forces, and each plane is formed by covalently bonded in-plane S−Mo−S atoms (see Figure 1a). Therefore, micromechanical exfoliation can be used to fabricate and isolate atomically thin MoS_2 thin sheets.[14,15]

While the band gap (∼1.29 eV) is indirect in multilayer MoS_2, it has been demonstrated that it becomes direct (∼1.8 eV) for a single-layer MoS_2.[7] The presence of significant band gap, coupled with high thermal stability and electrostatic integrity,[8] renders atomically thin MoS_2 as a new competitor to graphene as well as traditional semiconductors in a variety of applications, such as low-power field effect transistors (FET).[8] However, large variations in transport properties, presumably due to extrinsic/environmental effects, are often observed for MoS_2 devices, which limits one from exploring their intrinsic properties and overall stability. In fact, the field effect mobility of atomically thin MoS_2 FET has been reported to vary from 0.5 to 320 $cm^2\ V^{-1}\ s^{-1}$, and on/off ratio can span several orders of magnitude.[8,14,16,17]

It is of significant scientific as well as technological importance to investigate the various possible factors that can influence the reliability of atomically thin MoS_2 devices, such as the field effect transistor. Similar to other low-dimensional semiconductors, atomically thin MoS_2 is likely to be highly sensitive to external chemical environment and illumination conditions, which in turn can be exploited as nanoscale chemical and photosensors. However, such effects are clearly undesirable for MoS_2-based FETs and related electronic device architecture and should be minimized or eliminated in order to improve the device reliability and stability. Herein, we have fabricated atomically thin MoS_2 FETs and tested their performance under different humidity and illumination conditions. Both hysteretic and transient behaviors in conductance characteristics were observed, and further analysis suggests that the hysteresis in MoS_2 FET devices is largely due to absorption of moisture and high photosensitivity of MoS_2,

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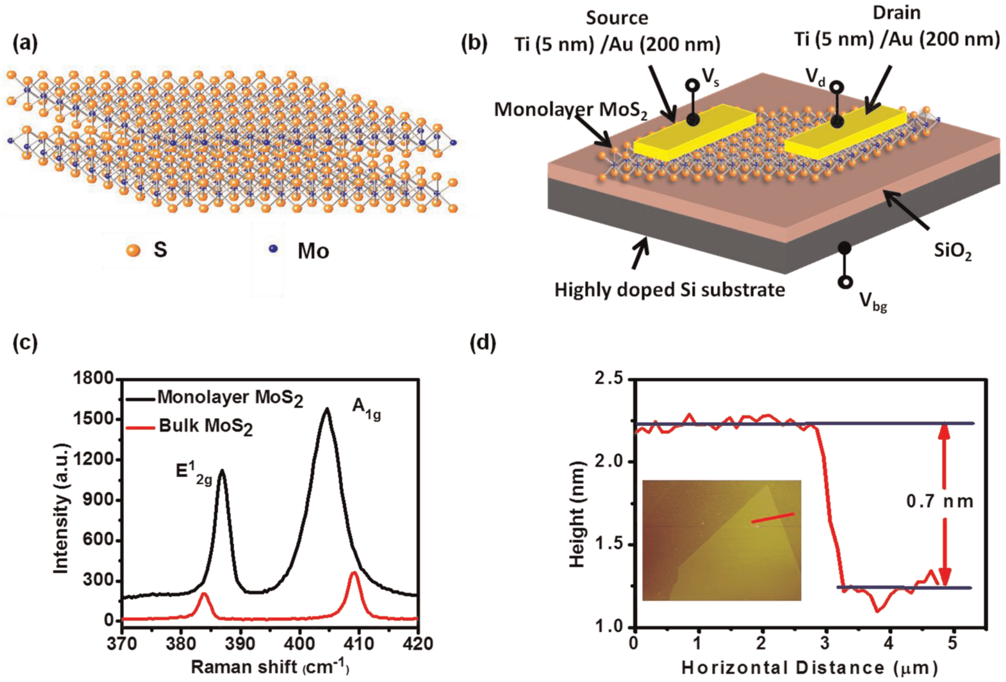

Figure 1. Structure and characterization of atomically thin MoS_2. (a) Three-dimensional schematic of the atomic structure of MoS_2. (b) Schematic representation of single-layer MoS_2 FET with highly doped silicon as the back gate. (c) Raman shift as a function of MoS_2 layer number. (d) AFM height profile of monolayer MoS_2; inset is the corresponding AFM image.

which should be addressed but have hitherto received inadequate attention. Furthermore, we demonstrate that nearly "*hysteresis-free*" FETs with enhanced mobility can be obtained by uniformly encapsulating the as-made devices with amorphous silicon nitride (Si_3N_4) coating.

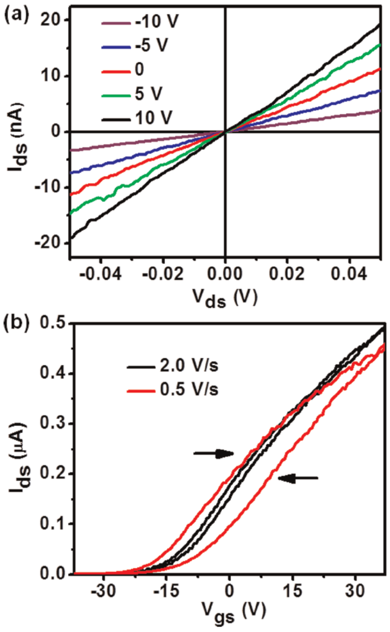

Figure 2. Transport properties of one single-layer MoS_2 transistor in the ambient environment at 24 °C and 12% RH. (a) $I_{ds}-V_{ds}$ characteristics at different fixed gate biases. (b) Hysteretic behavior of $I_{ds}-V_{gs}$ at fixed drain-source bias with different sweeping rates of the gate voltage. Hysteresis changes from 2 to 15 V as the sweeping rate slows from 2 to 0.5 V/s. Arrows indicate the gate bias sweep direction.

RESULTS AND DISCUSSION

Atomically thin MoS_2 flakes were prepared by micromechanical exfoliation of bulk MoS_2 crystals on highly doped silicon substrate covered with a thin layer of thermal oxide SiO_2. As we reported previously, optical contrast of these flakes was correlated with atomic force microscopy (AFM) and Raman spectroscopy to determine the exact thickness and number of layers in the thin flakes.[15] In Figure 1c, we show the shift of peak position of E^1_{2g} and A_{1g} modes in Raman spectra from MoS_2 bulk to monolayer film. Corresponding AFM and height profile (see Figure 1d) confirm the single-layer nature. The electrical contacts on MoS_2 were fabricated by electron beam lithography and electron beam evaporation of Ti (5 nm)/Au (150 nm) (see Figure 1b for the three-dimensional scheme of MoS_2 FET device and Figure S1 in the Supporting Information for the SEM image of a fabricated device). All two-probe transport measurements were carried out at room temperature in air under uniform white illumination (radiant flux density ~0.7 mW cm^{-2}), if not specified otherwise. Here, white illumination is used to reduce contact resistance, and its effect on the transport property of MoS_2 FET will be addressed in detail later. At low voltages, $I_{ds}-V_{ds}$ is almost linear at all V_{gs} (see Figure 2a), where I_{ds}, V_{ds}, and V_{gs} are the drain-source current and voltage and gate bias, respectively. These results resemble the transport characteristics at low voltage reported elsewhere.[11,17] However, these atomically thin MoS_2 flakes typically show nonlinear

$I_{ds}-V_{ds}$ characteristics at higher bias voltages, as shown in Figure S2 in Supporting Information. The near-symmetrical nonlinear nature of $I_{ds}-V_{ds}$ can be explained by the formation of back-to-back Schottky diodes in the metal–semiconductor–metal (M–S–M) structure with similar Schottky barrier heights at both ends, as shown for other low-dimensional semiconductor devices.[18,19]

The gating characteristics $I_{ds}-V_{gs}$ at constant V_{ds} = 0.5 V is shown in Figure 2b, from which we extracted the field effect mobility using the equation

$$\mu = \frac{1}{C_i}\frac{L}{W}\frac{dI_{ds}}{dV_{gs}}\frac{1}{V_{ds}} \qquad (1)$$

where C_i is the capacitance per unit area between the conducting channel and the back gate ($C_i = \varepsilon_0\varepsilon_r/d$; ε_r = 3.9 for SiO_2; d is the thickness of insulating layer SiO_2, 300 nm), L is the channel length (~1 μm), W is the channel width (from 2 to 10 μm for various devices). The typical field effect mobility of the as-made devices varies from 1.1 to 10 $cm^2\ V^{-1}\ s^{-1}$, and on/off ratio can vary up to 10^6. These devices are comparable to other back-gated MoS_2 FETs without dielectric screening in the references.[10,11,13]

All of the investigated devices exposed to the ambient environment conformed to depletion-like mode with negative threshold voltage and exhibited repeatable hysteresis in $I_{ds}-V_{gs}$ characteristics when V_{gs} was swept from −37 to 37 V and back to −37 V (see Figure 2b). The change of gate bias sweeping direction from forward to backward induced a noticeable positive threshold voltage shift up to ~25 V and reduced drain-source current. The hysteresis, defined as the magnitude of the threshold voltage shift, depends significantly on gate bias sweeping rate. As shown in Figure 2b, the hysteresis increased from 2 to 15 V as the sweeping rate slowed from 2 to 0.5 V/s. Hysteretic behavior has been observed in a variety of traditional semiconductor FETs and novel low-dimensional devices, like ZnO nanowire,[20] carbon nanotube,[21,22] and graphene FET.[23,24] Charge injection at the interfaces between semiconductor and substrate and charge transfer from/to neighboring adsorbates have been attributed as two possible factors in charge trapping and thus the resultant hysteresis.[23] However, considering the thickness of the SiO_2/Si substrate and uniform electrical field between two-dimensional MoS_2 film and the substrate, the possibility of local breakdown of SiO_2 and thus charge injection into the substrate is much lower than that of charge transfer from/to absorbed molecules like water, the most abundant dipolar adsorbate under ambient condition.[22] In fact, water absorption has been studied for a long time to explain the decreasing lubricant effectiveness of MoS_2.[25] Besides water, oxygen has also been considered as the cause of hysteresis, as in ZnO nanowire FETs.[20] However, in such kind of metal oxide semiconductors, oxygen can only affect the hysteresis through the balance with oxygen vacancies. In the case of MoS_2, its effect should likely be relatively small, which would also be tested in this paper.

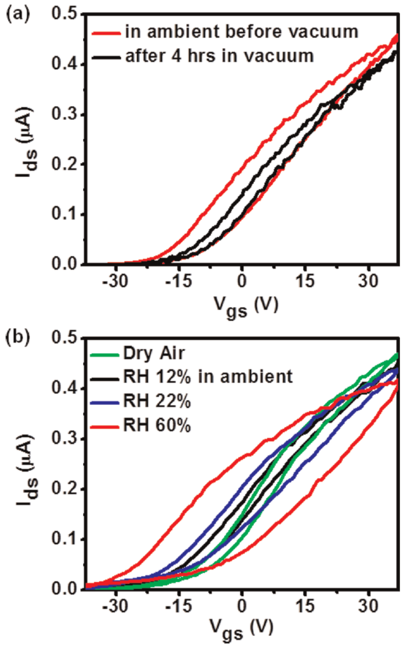

Figure 3. Hysteresis in the single-layer MoS_2 transistor with heat treatment in vacuum and controlled humidity under the same sweeping rate of gate voltage at 0.5 V/s and V_{ds} = 0.5 V. (a) Device exhibits reduced hysteresis (black curve, ~5 V) under low vacuum (~3 in. Hg) after vacuum heating at 3 in. Hg and 90 °C. The red line is the hysteresis of the device in ambient before vacuum treatment. (b) Hysteresis evolution of same device under different humidity. In dry air, small but finite hysteresis is likely due to the residual moisture at the interface between MoS_2 and substrate. Here, the current at V_{gs} = 37 V is the largest, which indicates relatively slow decay and smaller density of charge trapping states. With increase in humidity, hysteresis grows larger and steadily from 4 V (12% RH, black curve) to 15 V (22% RH, blue curve) and finally to 25 V (60% RH, red curve); the current at V_{gs} = 37 V steadily decreases, which indicates the growing decay rate and higher density of charge trapping states.

In order to confirm the humidity-related hysteresis, a series of control experiments under different chemical environment were conducted. The sample was first placed in vacuum oven with low vacuum (~3 in. Hg) and flushed with H_2/Ar (10% v/v) three times and heated for 4 h at 90 °C and then cooled to room temperature under the same vacuum. The measured hysteresis was reduced to 5 V (see black curve in Figure 3a). These observations indicate that hysteresis is mainly due to ambient molecules absorbed to the surface of MoS_2, such as water or oxygen. In order to eliminate the possibility of oxygen interference, we have tested device performance in dry air (green curve in Figure 3b, stabilization time was 30 min for dry air and other humidity conditions). No large difference was observed in comparison with hysteresis in vacuum, and therefore, oxygen is unlikely to be a significant contributor

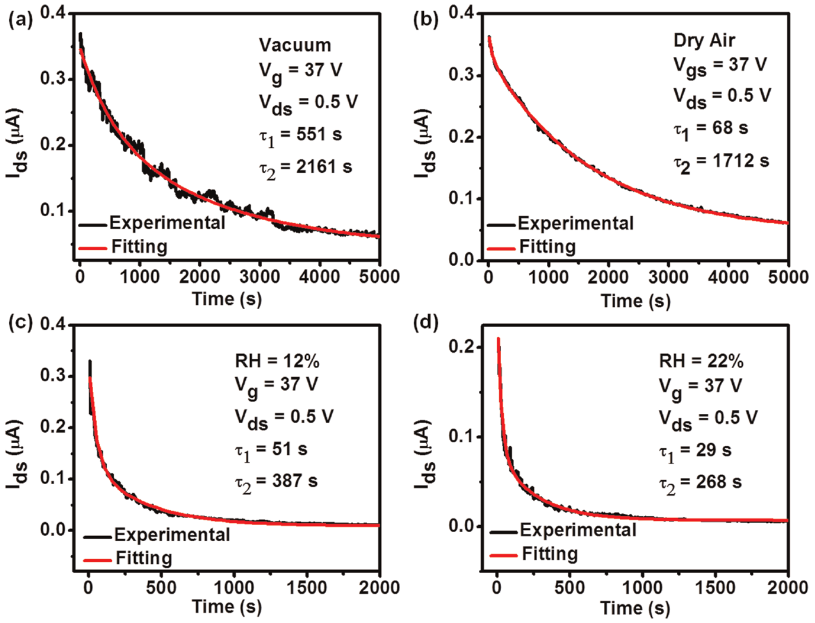

Figure 4. Transient property of the single-layer MoS_2 transistor under controlled humidity conditions and data fitting with biexponential equation. (a) Under vacuum, the decay of drain current is noticeably slow. (b) In dry air, the device still exhibits slow decay and large time constants. (c) At RH = 12%, drain current decays dramatically with rather small time constants. (d) With the increase of RH up to 22%, the current decay accelerates further.

to the hysteresis in atomically thin MoS_2 FETs. Meanwhile, relatively small hysteresis still observed in both vacuum and dry air could be related to residual water at the interfaces between MoS_2 and SiO_2. It is well-known that silanol-bound water on SiO_2 cannot be fully removed by heating below 200 °C,[26] which is simply beyond the scope of the vacuum oven used here. With higher relative humidity (RH), the hysteresis steadily increased, as shown in Figure 3b, from 4 V (12% RH, black curve) to 15 V (22% RH, blue curve) to 25 V (60% RH, red curve), while the current at V_{gs} = 37 V decreased accordingly. This is possibly due to a higher density of trapping states induced by increased humidity and thus faster charge transfer and current decay.

As evidence of this humidity-related current decay, the transient property of drain-source current at fixed V_{ds} = 0.5 V and V_{gs} = 37 V was investigated under the same controlled humidity condition (see Figure 4). In order to quantify the trapping time constant, we find that transient data could be fit excellently with a biexponential equation of the type

$$I = I_0 + Ae^{-t/\tau_1} + Be^{-t/\tau_2} \qquad (2)$$

where τ_1 and τ_2 are two relaxation time constants, possibly corresponding to two different trapping mechanisms. Under vacuum (Figure 4a), I_{ds} decayed exponentially from 0.37 μA in time and saturated after 5000 s with large time constants, τ_1 = 551 s and τ_2 = 2161 s. In dry air (Figure 4b), the exponential decay still exhibited large time constants of 68 and 1712 s, respectively. Once exposed to higher humidity (12% for Figure 4c and 22% for Figure 4d), the device showed even faster decay of current with dramatic decrease of time constants to one-tenth of those in vacuum. Clearly, higher humidity induced smaller time constants and more rapid current decay. These time constants from tens of seconds to thousands indicate that carrier trapping, responsible for hysteresis, is a rather slow phenomenon in MoS_2-based FET exposed to ambient environment.[20,24] Therefore, only when the sweeping rate is comparable to this slow charge trapping process, appreciable effects can be observed in the hysteresis.

Though the underlying mechanism of absorbed water molecules on hysteretic behavior is still not fully understood and requires further investigation, one possible explanation is that hysteresis could be due to the large electric dipole of water molecules (~1.8 D). In the case of monolayer MoS_2 FETs, the back-gate-induced electric field can be up to 100 MV/m. Water molecules could easily respond to the field and be aligned. Such alignment of polar water molecules under sweeping gate bias probably imposes various dipole fields to the channel of the FETs and induces different charge trap densities, which could explain the hysteresis and transient behavior in atomically thin MoS_2 FETs. In comparison with hydrophobic graphene, the sulfur surface of MoS_2 has a significant polarity and hydrophilicity, which absorbs water rather easily through formation of hydrogen bond, for example, Mo—S···H—O—H, and the number of hydrogen bonds corresponds proportionally to the amount of adsorbed water which is related to the humidity.

Such effect has already been studied to explain the effectiveness change of MoS_2 lubricant.[25] Moisture absorption is also consistent with a recent study on ALD growth of uniform Al_2O_3 on the MoS_2 surface, where H_2O is one of the precursors and physical absorption is attributed to the feasibility of direct ALD growth.[27] Therefore, exposure of MoS_2 to ambient air with higher humidity causes a larger amount of absorbed water molecules and induces charge traps and thus eventually increases hysteresis in FETs.

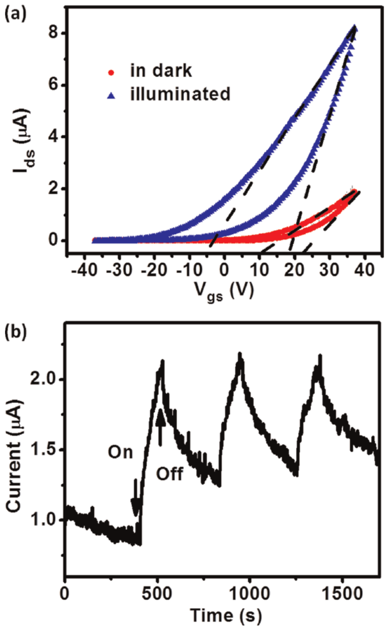

Figure 5. (a) Hysteresis with different illumination conditions in a single-layer MoS_2 transistor. Blue dots are under global white illumination (0.7 mW/cm^2), and red dots are in the dark. The intersections between the dashed lines and y = 0 show the threshold voltages. (b) Photoresponse of the same device at V_{ds} = 2 V, V_{gs} = 0 V. Illumination was on for 2 min, then off for 5 min, and the period was repeated three times.

Besides humidity, hysteretic behavior was investigated under different ambient illumination conditions, either under white illumination (radiant flux density ~0.7 mW cm^{-2}) or in the dark. The devices showed significant photosensitivity, as reported recently.[4] Figure 5a shows that the device was switched to enhancement-like mode in the dark, as the threshold voltage moves to the positive side in both sweeping directions, and the decrease of drain current from illumination to dark at zero gate voltage is up to 2 orders of magnitude. More strikingly, the hysteresis is dramatically suppressed, as the change of threshold voltage in hysteresis goes further down to 10 V from 20 V under white illumination. If the above-mentioned water-induced charge transfer model holds here, the reduced hysteresis is not difficult to understand: charge traps induced by absorbed water are occupied by electrons transferred from MoS_2; as the illumination is turned off, the carrier concentration in the channel decreases and hence the charge transfer is suppressed.

To further confirm this photosensitivity of MoS_2, the response of the device to uniform white illumination at zero gate bias was recorded at room temperature (see Figure 5b). The aforementioned results show that MoS_2 is highly sensitive to white illumination. Because MoS_2 is a narrow band gap semiconductor, ambient

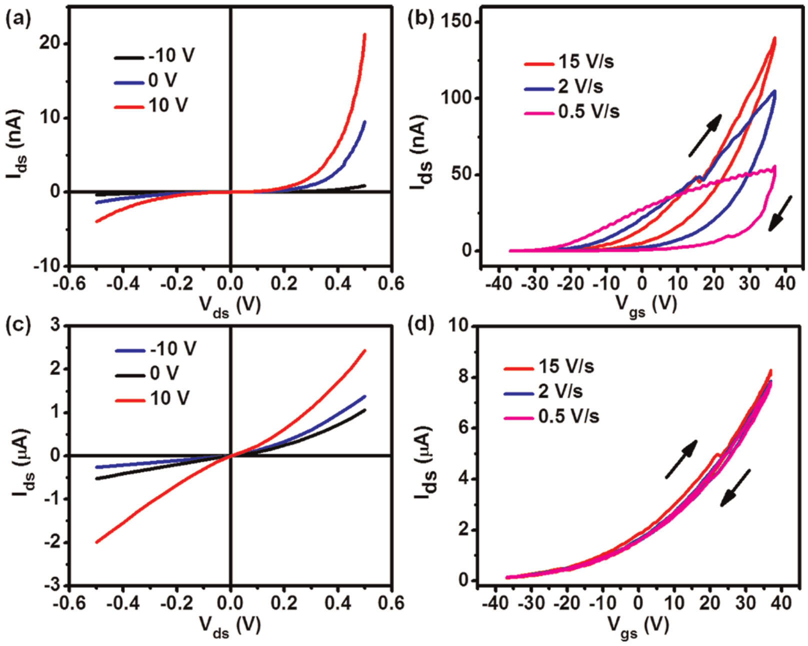

Figure 6. Effect of device passivation with PECVD-grown Si_3N_4. Before passivation: (a) $I_{ds}-V_{ds}$ characteristics at different fixed gate biases. (b) Hysteretic behavior of $I_{ds}-V_{gs}$ at fixed drain-source bias with different sweeping rates of the gate voltage. After passivation: (c) $I_{ds}-V_{ds}$ characteristics at different fixed gate biases became more linear and the conductivity was improved. (d) Hysteretic behavior of $I_{ds}-V_{gs}$ is almost removed even at slow scan rate such as 0.5 V/s.

illumination used in most of device tests and its intensity fluctuation should explain the unexpected variance of device properties. Therefore, in order to reduce its effect, the illumination should be well-controlled and stabilized for sufficiently long time.

Furthermore, we demonstrate that coating MoS_2 devices with amorphous Si_3N_4 can largely eliminate the hysteresis and simultaneously enhance the mobility by 1 order of magnitude. This was achieved by depositing Si_3N_4 by plasma-enhanced chemical vapor deposition (PECVD) onto the as-made MoS_2 transistors. The as-made devices were first heated up to 300 °C at 5 mTorr in 1 h to remove moisture absorbed on the surface. Then Si_3N_4 thin films were deposited at 300 °C and 320 mTorr using NH_3 (40 sccm) and 10% SiH_4 in N_2 (100 sccm) with a plasma power of 15 W. The devices were tested under high humidity (RH $\sim$ 60%) before and after Si_3N_4 passivation. Before passivation, a MoS_2 transistor exhibited nonlinear $I_{ds}-V_{ds}$ characteristics (Figure 6a) and serious hysteresis in $I_{ds}-V_{gs}$ (Figure 6b), as expected previously. With a 30 nm Si_3N_4 passivation layer, the conductivity of the same transistor dramatically increased by over 100 times, which means that the contact between MoS_2 and the electrode should be improved during the high-temperature vacuum heating. What is more important is that the device became nearly hysteresis-free at various gate bias sweeping rates under high humidity, and the mobility was enhanced by over 1 order from 1.7 to 71.8 $cm^2\ V^{-1}\ s^{-1}$, which could be due to the improved contact and suppressed Coulomb scattering *via* dielectric screening as confirmed in graphene FETs.[28,29]

Compared to other kinds of passivation layers, such as PMMA,[22] SiO_2,[30] and HfO_2,[31] the advantages of Si_3N_4 are (1) uniform coverage with no visible pinholes is easily obtained with PECVD-grown Si_3N_4, as shown in AFM images of the passivated device in Supporting Information; (2) growth environment is mildly reducing in NH_3, and there is no risk of oxidizing MoS_2 ultrathin films during deposition; (3) Si_3N_4 thin films are relatively dense, which can prevent water penetration into the devices; (4) growth at 300 °C and high vacuum can remove all of the absorbed water from both MoS_2 surface and the interface between MoS_2 and the substrate. Further improvement is under investigation and will be discussed in the following paper.

CONCLUSION

In summary, we targeted the origin of the observed hysteresis in atomically thin MoS_2 FET: (1) trapping states induced by absorbed water molecules on MoS_2 surface is the primary factor; and (2) photosensitivity of MoS_2 can significantly increase the hysteresis when MoS_2 FET is exposed to white illumination. In order to reduce the hysteretic effect and enhance the device mobility, vacuum heating and hermetic passivation with Si_3N_4 thin film was carried out. Besides, well-controlled and stable illumination condition during the test is critical to obtain repeatable and comparable results. The current work also indicates that controllable hysteretic behavior in MoS_2 FETs has the potential for humidity sensors[22] and nonvolatile memory devices,[32] while the high photosensitivity of MoS_2 and its application as photodetectors needs to be further explored.

METHODS

Atomically Thin MoS_2 Sample Preparation. Atomially thin MoS_2 flakes were deposited at room temperature in ambient condition by mechanically exfoliating bulk MoS_2 materials (SPI Supplier, USA) onto SiO_2 (300 nm)/Si substrates in a manner similar to that previously established for single-layer graphene. The thinnest flakes were identified by optical microscopy. The exfoliated flakes had typical dimensions of tens of micrometers. The as-synthesized MoS_2 single-layer and few-layer samples were characterized by optical microscopy, AFM (Bruker ICON), and Raman spectroscopy system (Nanophoton Raman-11). In Raman spectroscopy, the 532 nm line of an Ar ion laser was used as the excitation source with a laser power of ~1 mW. The laser beam was focused onto the dispersed sample by a 100× microscope objective lens, and the scattered light was collected in the backscattering geometry. The collected scattered light was dispersed by a spectrometer grating of 2400 mm and was detected with an electrically cooled CCD detector. The spatial resolution was less than 0.8 μm, and the spectral resolution was 1.6 cm^{-1} with peak position accuracy of 0.1 cm^{-1}.

MoS_2 Field Effect Transistor Device Fabrication. After identifying atomically thin MoS_2, we fabricated the electrodes using electron beam lithography. First, the samples were spin-coated with MMA (8.5) and MAA (6% concentration in ethyl lactate), baked at 180 °C for 1 min, then coated with PMMA (2% concentration in anisole) followed by baking at 180 °C for 1 min and exposed by a focused 30 keV electron beam in FEI Quanta ESEM. After development in MIBK, IPA 1:3 solution for 60 s, we evaporated contact materials (Ti/Au, 5/150 nm thickness) and did lift-off in acetone.

Electrical Characterization. The heavily doped silicon substrate was used as the back gate. Electrical characterization of atomically thin MoS_2 field effect transistor devices was carried out using a Keithley 4200 semiconductor characterization system with a shielded probe station with micromanipulator in ambient air with a top lamp to provide global white illumination at 0.7 mW cm^{-2}. The humidity control experiments were conducted in a vacuum oven, which can be pumped to low vacuum ~3 in. Hg and heated up to 90 °C. Before each measurement, the device was allowed for 30 min to stabilize.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: SEM image of a MoS_2 FET device, nonlinear $I-V$ characteristics of the device, and optical and AFM images of a Si_3N_4-passivated device. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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